```
=> d hist


      (FILE 'USPAT' ENTERED AT 14:15:49 ON 18 MAY 1998)
L1         8335 S EMULAT###
L2           37 S L1 AND DEBUG####(10A)(FIFO OR QUEUE OR BUFFER#)
L3          579 S L1 AND DEBUG#### AND TRAC###
L4          281 S L3 AND INTERFAC###(10A)BUS##
L5          247 S L4 AND (ICE OR CIRCUIT)
L6           27 S L5 AND (395*500 OR 395*527 OR 395*385)/CCLS
L7           35 S L2 NOT L6
L8           27 S L5 AND L6
L9            2 S L2 AND L6

=> d 16 cit 6 8 9 10 20 21
```

now U.S

6. 5,630,102, May 13, 1997, In-**circuit-emulation** event management system; Thomas M. Johnson, et al.,**395/500** [IMAGE AVAILABLE]

8. 5,594,890, Jan. 14, 1997, **Emulation** system for **emulating** CPU core, CPU core with provision for **emulation** and ASIC having the CPU core; Shinichi Yamaura, et al., **395/500**; 364/578; 371/22.5, 22.6 [IMAGE AVAILABLE]

9. 5,564,041, Oct. 8, 1996, Microprocessor for inserting a bus cycle in an instruction set to output an internal information for an **emulation**; Shigezumi Matsui, et al., **395/500**; 364/232.3, 232.8, 264.1, 264.2, 264.5, 267, DIG.1; 395/740 [IMAGE AVAILABLE]

10. 5,546,562, Aug. 13, 1996, Method and apparatus to **emulate** VLSI circuits within a logic simulator; Chandresh Patel, **395/500**; 364/488, 578, DIG.1; 395/183.04, 183.09 [IMAGE AVAILABLE]

20. 5,321,828, Jun. 14, 1994, High speed microcomputer in-**circuit emulator**; Michael D. Phillips, et al., **395/500**; 364/232.3, 264.3, DIG.1 [IMAGE AVAILABLE]

21. 5,313,618, May 17, 1994, Shared bus in-**circuit emulator** system and method; Martin B. Pawloski, **395/500**; 364/DIG.1, DIG.2; 395/183.04, 183.05 [IMAGE AVAILABLE]

```
=> d 17 cit 6 7
```

6. 5,710,934, Jan. 20, 1998, Methods and test platforms for developing an application-specific integrated circuit; Mariano Bona, et al., 395/183.06 [IMAGE AVAILABLE]

7. 5,680,583, Oct. 21, 1997, Method and apparatus for a trace buffer in an **emulation** system; Han Kuijsten, 395/500 [IMAGE AVAILABLE]

```
=> d 19 cit 2
```

2. 5,321,828, Jun. 14, 1994, High speed microcomputer in-**circuit emulator**; Michael D. Phillips, et al., 395/500; 364/232.3, 264.3, DIG.1 [IMAGE AVAILABLE]

```
=> d hist


        (FILE 'USPAT' ENTERED AT 14:15:49 ON 18 MAY 1998)
L1         8335 S EMULAT###
L2           37 S L1 AND DEBUG####(10A)(FIFO OR QUEUE OR BUFFER#)
L3          579 S L1 AND DEBUG#### AND TRAC###
L4          281 S L3 AND INTERFAC###(10A)BUS##
L5          247 S L4 AND (ICE OR CIRCUIT)
L6           27 S L5 AND (395*500 OR 395*527 OR 395*385)/CCLS

=> d l6 cit 1-27
```

1. 5,721,879, Feb. 24, 1998, **Emulator** dedicated one-chip
microcomputer; Hisashi Harada, et al., **395/500** [IMAGE AVAILABLE]

2. 5,701,502, Dec. 23, 1997, Isolating a central processing unit from
the operating system controlling said unit and its associated hardware
for interaction of the unit with data handling apparatus alien to the
operating system; Ernest Dysart Baker, et al., **395/500**, 200.31, 290,
406, 680 [IMAGE AVAILABLE]

3. 5,687,371, Nov. 11, 1997, Selection from a plurality of **bus**
operating speeds for a processor **bus interface** during processor
reset; Phillip G. Lee, et al., 395/651, 309, **500**, 568 [IMAGE
AVAILABLE]

4. 5,684,721, Nov. 4, 1997, Electronic systems and **emulation** and
testing devices, cables, systems and methods; Gary L. Swoboda, et al.,
364/578, 488, 489; **395/500** [IMAGE AVAILABLE]

5. 5,640,541, Jun. 17, 1997, Adapter for **interfacing** a SCSI **bus**
with an IBM system/360/370 I/O **interface** channel and information
system including same; Robert P. Bartram, et al., **395/500** [IMAGE
AVAILABLE]

6. 5,630,102, May 13, 1997, In-**circuit-emulation** event
management system; Thomas M. Johnson, et al., **395/500** [IMAGE
AVAILABLE]

7. 5,603,012, Feb. 11, 1997, Start code detector; Martin W. Sotheran,
395/500; 370/450 [IMAGE AVAILABLE]

8. 5,594,890, Jan. 14, 1997, **Emulation** system for **emulating** CPU
core, CPU core with provision for **emulation** and ASIC having the CPU
core; Shinichi Yamaura, et al., **395/500**; 364/578; 371/22.5, 22.6
[IMAGE AVAILABLE]

9. 5,564,041, Oct. 8, 1996, Microprocessor for inserting a bus cycle in
an instruction set to output an internal information for an
emulation; Shigezumi Matsui, et al., **395/500**; 364/232.3, 232.8,
264.1, 264.2, 264.5, 267, DIG.1; 395/740 [IMAGE AVAILABLE]

10. 5,546,562, Aug. 13, 1996, Method and apparatus to **emulate** VLSI
circuits within a logic simulator; Chandresh Patel, **395/500**; 364/488,
578, DIG.1; 395/183.04, 183.09 [IMAGE AVAILABLE]

11. 5,530,804, Jun. 25, 1996, Superscalar processor with plural

pipelined execu[ ]n units each unit selectively h[ ]ving both normal and
debug modes; Gr[ ]ry C. Edgington, et al., 395/1[ ]06, **500**,
800.23, 800.43 [IMAGE AVAILABLE]

12.   5,438,674, Aug. 1, 1995, Optical disk system **emulating** magnetic
tape units; Richard V. Keele, et al., 711/4; 364/927.81, 952.31, 952.6,
955.5, 961.2, DIG.2; **395/500**; 707/204, 205; 711/112, 202, 221 [IMAGE
AVAILABLE]

13.   5,408,637, Apr. 18, 1995, **Emulation** techniques giving necessary
information to a microcomputer to perform software **debug** and system
debug even for incomplete target system; Hisayoshi Shimizu,
395/500; 364/578, 927.81, DIG.2 [IMAGE AVAILABLE]

14.   5,392,420, Feb. 21, 1995, In **circuit emulator**(ICE) that
flags events occuring in system management mode(SMM); Mark Balmer, et
al., **395/500**; 364/260.8, DIG.1; 395/800.43 [IMAGE AVAILABLE]

15.   5,390,356, Feb. 14, 1995, Rapid reprogramming terminal; Christian L.
Houlberg, **395/500**; 364/242.5, 260, 942, 942.3, DIG.1, DIG.2 [IMAGE
AVAILABLE]

16.   5,388,215, Feb. 7, 1995, Uncoupling a central processing unit from
its associated hardware for interaction with data handling apparatus
alien to the operating system controlling said unit and hardware; Ernest
D. Baker, et al., 395/200.59; 364/232.3, 280, DIG.1; 395/200.51, 200.57,
500 [IMAGE AVAILABLE]

17.   5,371,878, Dec. 6, 1994, System for analysis of embedded computer
systems; Robert T. Coker, **395/500**; 364/260.4, 264.3, 267.91, DIG.1
[IMAGE AVAILABLE]

18.   5,349,685, Sep. 20, 1994, Multipurpose **bus interface**
utilizing a digital signal processor; Christian L. Houlberg, 395/800.4;
364/240.5, 240.7, 240.8, 259.9, DIG.1; **395/500**, 800.37 [IMAGE
AVAILABLE]

19.   5,329,471, Jul. 12, 1994, **Emulation** devices, systems and methods
utilizing state machines; Gary L. Swoboda, et al., 364/578, 264.3, 264.5,
267.4, 267.7, DIG.1; 371/22.32; 395/183.04, 183.06, **500** [IMAGE
AVAILABLE]

20.) 5,321,828, Jun. 14, 1994, High speed microcomputer in-**circuit
emulator**; Michael D. Phillips, et al., **395/500**; 364/232.3, 264.3,
DIG.1 [IMAGE AVAILABLE]

21.   5,313,618, May 17, 1994, Shared bus in-**circuit emulator**
system and method; Martin B. Pawloski, **395/500**; 364/DIG.1, DIG.2;
395/183.04, 183.05 [IMAGE AVAILABLE]

22.   5,289,587, Feb. 22, 1994, Apparatus for and method of providing the
program counter of a microprocessor external to the device; Bruce B.
Razban, **395/500**; 364/247.8, 267.91, 285, DIG.1; 395/184.01 [IMAGE
AVAILABLE]

23.   5,283,868, Feb. 1, 1994, Providing additional system characteristics
to a data processing system through operations of an application program,
transparently to the operating system; Ernest D. Baker, et al.,
395/200.57; 364/228.7, 228.9, 229, 229.1, 230, 230.3, 232.1, 232.3, 238,
238.4, 239, 240, 240.5, 240.8, 240.9, 241.2, 241.9, 242.3, 242.31, 242.6,
242.94, 242.95, 243, 243.4, 246, 246.3, 247, 247.3, 251, 254, 254.3,
254.5, 256.3, 256.4, 258, 259, 259.2, 264, 265, 268, 268.9, 270, 271,
273.4, 280, 280.2, 280.8, 281.3, 282.1, 282.4, 284, 284.3, DIG.1;
395/200.76, **500** [IMAGE AVAILABLE]

24.   5,140,687, Aug. 18, 1992, Data processing apparatus with

self-**emulation** ●ability; Thomas A. Dye, et al. ●395/500 [IMAGE AVAILABLE]

25. 5,088,033, Feb. 11, 1992, Data processing system **emulation** in a window with a coprocessor and I/O **emulation**; Joseph H. Binkley, et al., **395/500**; 364/222.81, 228.2, 228.6, 231, 232.3, 234, 236.2, 237.2, 237.3, 238, 238.3, 238.6, 238.9, 239, 239.6, 239.9, 240, 241.2, 241.3, 241.6, 242.3, 242.31, 242.6, 242.92, 244, 244.6, 247, 247.2, 247.8, 248.1, 256.3, 256.6, 259, 259.9, 260, 260.1, 261.3, 261.9, 262.4, 262.9, 264, 264.3, 265, 266.6, 270, 271, 271.2, 271.5, 280, 280.2, 286.1, 286.3, DIG.1 [IMAGE AVAILABLE]

26. 5,056,015, Oct. 8, 1991, Architectures for serial or parallel loading of writable control store; David R. Baldwin, et al., **395/500**; 364/228.6, 230, 230.1, 230.5, 239, 239.2, 242.3, 242.31, 243, 243.41, 244, 244.5, 244.6, 247, 247.4, 247.8, 260, 262.4, 262.7, 262.8, DIG.1 [IMAGE AVAILABLE]

27. 4,453,211, Jun. 5, 1984, System bus for an **emulated** multichannel system; Martin Askinazi, et al., **395/500**; 364/222.2, 228.1, 228.5, 229, 229.2, 230, 230.1, 230.4, 232.3, 232.9, 238.3, 238.4, 239, 239.2, 239.6, 240, 240.1, 240.4, 241.2, 241.5, 241.9, 242.3, 242.6, 242.7, 242.92, 244, 244.9, 246, 246.3, 253, 253.1, 254.8, 263.3, 264, 264.3, 264.6, 265, 265.1, 268, 268.3, 268.7, 271, 271.2, 271.6, 271.8, 280, 280.6, 284, 284.3, 285, 285.4, DIG.1 [IMAGE AVAILABLE]